Active Virtual Ground— Single-Phase Transformerless Grid-Connected Voltage Source Inverter Topology

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***Abstract*—An efficient single-phase Transformerless grid-connected voltage source inverter topology by using the proposed active virtual ground (AVG) technique is presented. With the AVG, the conventional output *L* filter can be reconfigured to *LCL* structure without adding additional inductor. High-frequency differential mode current ripple can be significantly suppressed comparing to the available single-phase grid-connected inverter topologies. Additionally, strong attenuation to the high-frequency common-mode current is achieved. It is particularly important for some applications such as photovoltaic and motor drives. High efficiency can be achieved due to fewer components involved in the conduction loss. Cost of the magnetic device can be reduced since the required inductance of the filter becomes smaller. Performance of the proposed inverter has been evaluated analytically. Experimental verification is performed on a 1-kW, 400-V input, and 110-V/60-Hz output prototype.**

***Index Terms*—Common-mode (CM) current, differential-mode (DM) current, inverters, leakage current.**

I. Introduction

NOWADAYS, direct current (DC) energy sources and storage elements, such as photovoltaic (PV) and battery cells, become essential in the modern power systems [1], [2]. In order to feed DC energy to alternative current (AC) grid network, a grid-connected power electronics voltage source inverter (VSI) is generally used as an interface [3]. It converts dc voltage to ac voltage and delivers the energy from the dc sources to the ac grid. The most well-known topology is a nonisolated full-bridge (FB) inverter. It has a simple structure and low semiconductor losses as only two semiconductors conduct at any given time [4]. However, a simple grid-connected FB VSI has to use bipolar switching scheme (two-level switching scheme), otherwise, using unipolar switching scheme (USS) (three-level switching scheme) will induce a high-frequency (HF) common-Mode (CM) voltage to ac grid. Therefore, a lot of research works have been studying the issue [5]– [8]. Practically, the CM voltage generates a HF leakage current at ground terminal in a grid network which can trigger circuit breakers to shut down the whole network. Besides, dc sources such as PV and battery cells are sensitive to CM voltage which will reduce their life time and degrade their performance [9]. Using a line-frequency transformer as an isolating element to break the leakage current path between grid network and system is a conventional and simple method to avoid the CM voltage problems. But the transformer is bulky, expensive, and high loss. It is not a preferred solution nowadays. Tranformerless VSI topologies with unipolar modulation are more popular. But high CM current is a typical problem. In order to protect equipment and human, there are some industrial standards which limit the leakage current to a certain level, such as 300 mA [10], for commercial power electronics transformerless inverter.

For grid-connected applications, many manufacturers and researchers have proposed various methods to get rid of the leakage current problems with a simple transformerless FB inverter. The conventional method is to use the bipolar switching scheme [3], [11], however, the method leads to large current ripple at the output current and a high inductance value output inductor is required. Besides, all antiparallel diodes in the inverter have to be low in reverse recovery loss since they all are in HF commutation loops. Using MOSFET is not a good option due to its poor body diode [12]. IGBT can be used but the current tail causes relatively high turn-off loss [13]. In order to achieve the following features, several VSI topologies have been proposed in the last decade:

1) providing unipolar switching to reduce the inductances of output filter,
2) utilizing fast commutation cells, a MOSFET and an individual fast reverse recovery diode, e.g., SiC Schottky diode, to reduce switching losses of semiconductors, and
3) suppressing leakage current to satisfy the industrial standards.

First, H5 topology was successfully proposed to solve the CM voltage issues and utilized in commercial products [14]. The

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topology includes an additional power semiconductor switch, which is connected in series of the dc source and the FB inverter. Switching actions of the additional power switch are synchronized with the main HF switches in the FB inverter. As a result, the additional power switch breaks the leakage current path when the current is circulating in the main semiconductor switches during the freewheeling states. However, the additional switch has to be full voltage and current rated and it conducts the rated current of the inverter. It slightly reduces the overall system efficiency due the conduction loss on the additional switch. Second, HERIC topology is another topology which was successfully proposed and adopted by the industry [15]. The topology includes an additional path in parallel with the FB inverter. HERIC topology successfully disconnects the input dc source from the output ac grid network during the freewheeling state by conducting the additional path and turning-off the four switches in the FB inverter. As a result, HF CM voltage can be avoided theoretically. But it requires two more full voltage and current rated HF power semiconductor switches, e.g., IGBTs, to form a bidirectional blocking switch and it increases the component cost. Other topologies have been proposed to solve the same problems, such as hybrid frequency phase legs [16], H6-Type configuration [17]–[18], and neutral point clamped (NPC) type [19]. In principle, they are all based on the H5 and the HERIC concepts, adding semiconductors to break or to bypass the leakage current path in the circuit. But they require adding further more semiconductor devices. Third, virtual ground (VG) technology has been proposed for PV systems to solve the CM voltage issues by using a three-phase three-wire inverter with controlling a potential difference of its midpoint of dc input capacitors and an unconnected neutral terminal to be almost zero voltage [20], [21]. This method can effectively reduce the leakage current for three-phase inverters. A similar approach has been proposed for single-phase inverters that uses two capacitors to return HF components to the input dc side of the FB inverter [9], it is namely capacitor-center-tapped (CCT) technique. CCT technique can minimize the CM voltage, but it still feeds the HF differential mode (DM) current to the grid. A bulky inductor for filtering will be required. Apart from the mentioned three methods, connecting the neutral terminal to the dc input, such as connecting to the middle point [22], [23] and the negative point [24], [25], can also suppress the leakage current. However, they require higher voltage and current rating semiconductor devices since the topologies work as a half-bridge inverter or cascading buck–boost converters. Higher semiconductor cost and switching losses are the drawback.

A transformerless grid-connected inverter associated with active VG (AVG) topology is proposed in this paper to mitigate the HF CM voltage and reduce the HF DM current ripple concurrently. Two bidirectional blocking semiconductors and a capacitor form the AVG circuit which is connecting to the line terminal, the neutral terminal, and a terminal of the input dc link. Fig. 1 shows the configuration and connections of the system. The circuit always keeps one of the grid terminals connecting to the input dc link through the AVG capacitor, C_1. From HF equivalent circuit point of view, the AVG capacitor is a low impedance element and the dc-link seems always

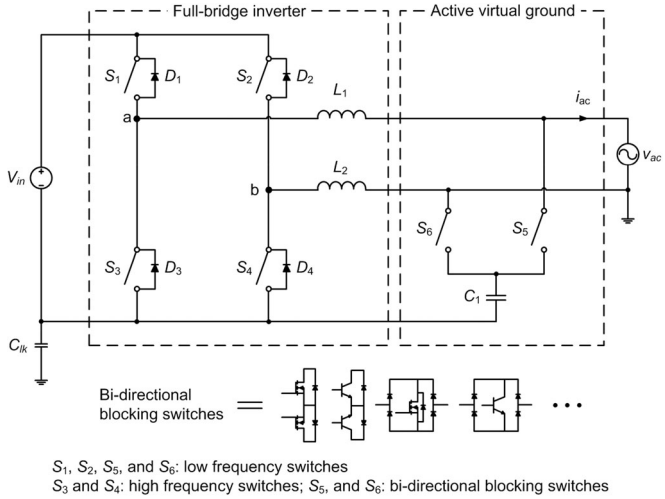

Fig. 1. Proposed single-phase transformerless FB inverter with AVG topology.

connecting to the network ground though the capacitor. Therefore, the technique is named AVG. This inverter topology has above three mentioned features. Additionally, it provides the following advantages:

1) The output filter is an *LCL* filter but without additional grid-side inductor. The output inductor of switching legs takes different roles, inverter-side inductor or grid-side inductor, in different operating modes. It further reduces the inductance of output inductors, grid current ripple amplitude, and the cost of inductors.
2) As only HF current components pass through the AVG circuit, additional conduction losses are minimized.

The paper will explain the operating principles of the proposed topology. Mathematical steady-state characteristics and a simplified design guideline of the proposed AVG circuit will be explained. Furthermore, benchmarking and variants of the proposed solution will be shown and discussed. The proposed topology is successfully demonstrated in a 1-kW, 400-V input, 110-Vrms/60-Hz ac grid-connected VSI prototype with a digital controller. The steady-state CM voltage characteristics of the VSI are studied. Experimental results show that the proposed inverter with AVG can effectively attenuate both HF CM and DM current ripples to the grid. The theoretical prediction and experimental results are in good agreement.

II. Operating Principle

A. Proposed Inverter Topology and HF DM Voltage Attenuation

Fig. 1 shows the circuit schematic of the proposed inverter with the AVG circuit. S_1– S_4, L_1, and L_2 form the ordinary single-phase FB inverter; S_5, S_6, and C_1 form the AVG circuit. Fig. 2 shows the gate signals of all the switches and output waveforms of the proposed inverter with USS at unity power factor condition. On the basis of switching scheme, S_1 and S_2 switch alternately at grid frequency (GF); S_3 and S_4 switch at HF, i.e., switching frequency, to shape the output current

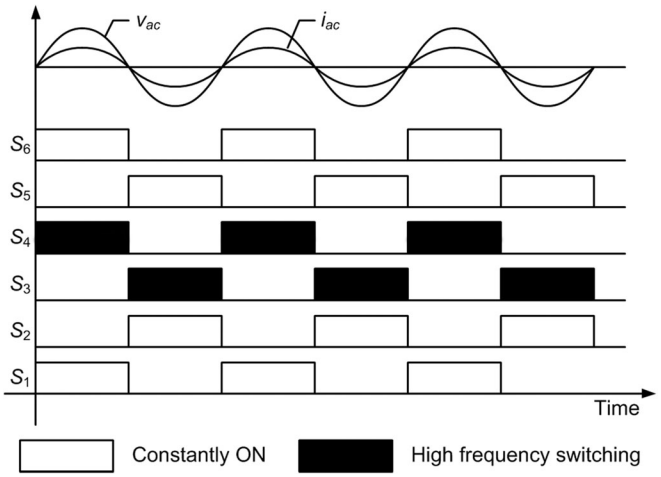

Fig. 2. Switching pattern of S_1–S_6 for unity power factor condition.

waveform as sinusoidal. Fig. 3(a) shows the operating mode for the positive half-line cycle. S_1 is constantly ON; S_4 is modulated by an average current mode controller and switched at HF. It can be inspected that an equivalent HF switching voltage source, namely v_b, with magnitude changing between V_{in} and zero is applied across node b and the negative terminal of V_{in}. As a result, an HF DM voltage with magnitude equal to V_{in} applies across the output inductors, L_1 and L_2, which creates large HF DM current ripple. Therefore, large inductance is required for L_1 and L_2 to suppress the current ripple which helps to lessen the EMI problem for inverter with the ordinary USS. The proposed AVG circuit aims to suppress the DM current ripple considerably in a way of reconfiguring the output filter form *L* to *LCL* structure. It is realized by synchronizing the switching actions of S_5 and S_6 with S_2 and S_1, respectively, for the case of unity power factor operation. By conducting S_6 and opening S_5 together with the aforementioned switching pattern among S_1– S_4, the output filter toward v_b will become an *LCL* structure in the positive half-line cycle. The HF equivalent circuit of the proposed inverter with AVG for positive half-line cycle is presented in Fig. 3(b). L_2, C_1, and L_1 form an *LCL* filter toward v_b. It can be observed that L_1 and L_2 act as the grid-side and the inverter-side inductors, respectively. As a result, attenuation to the HF DM voltage, as well as the HF DM current, by the output filter is 60 dB/decade. Most of the prior single-phase grid-connected inverter topologies cannot provide output *LCL* filter unless adding an additional grid-side inductor per phase leg. Therefore, the HF DM voltage attenuation of the proposed inverter with AVG is 40 dB/decade which is comparatively higher. A significant reduction on the required filter inductance is resulted for a given HF DM current ripple limit. S_5 and S_6 are bidirectional blocking switches and it can be implemented in different ways, some examples are shown in Fig. 1. Similarly, the HF equivalent circuit for the negative half-line cycle is shown in Fig. 3(c). An *LCL* output filter toward the HF switching voltage source, v_a, is formed by conducting S_5 and opening S_6. L_1 becomes the inverter-side inductor and L_2 acts as the grid-side inductor; S_2 is constantly ON and S_3 is switched at HF to shape the output current as sinusoidal.

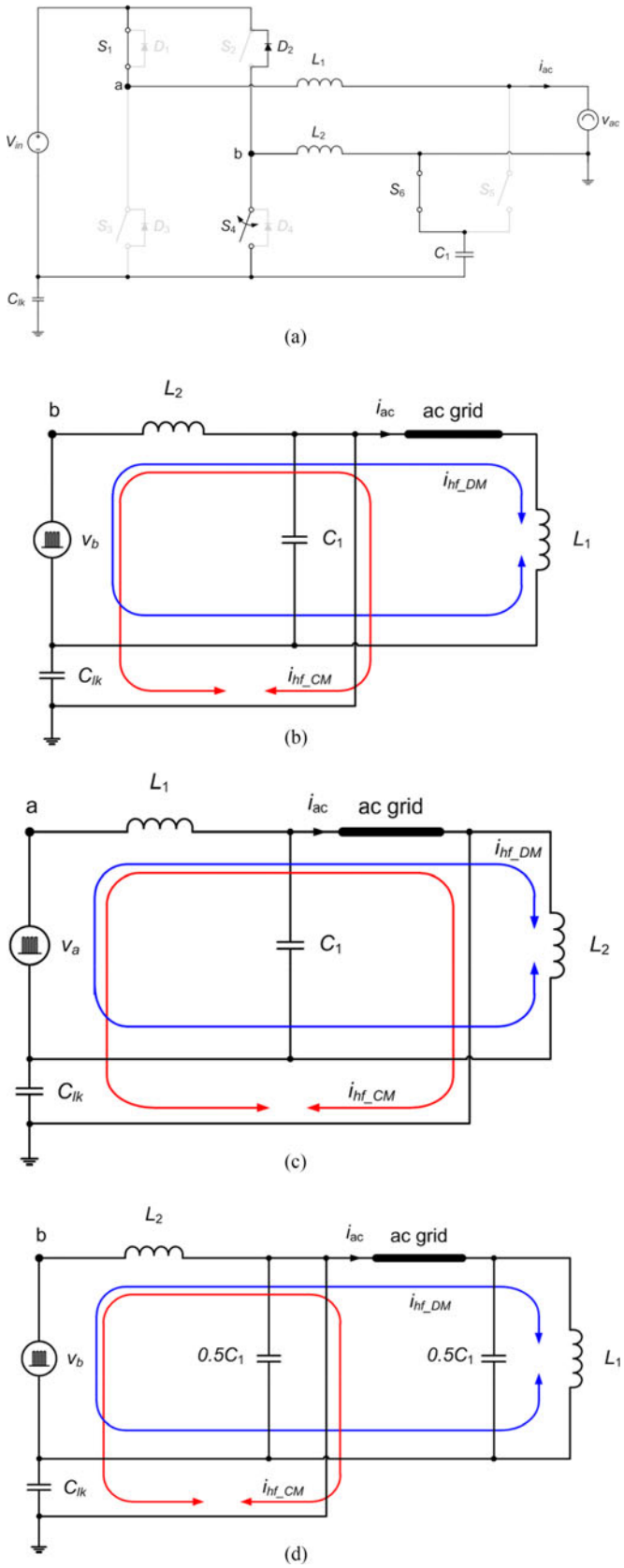

Fig. 3. Circuit diagram of (a) positive half-line cycle with AVG, (b) positive half-line cycle HF equivalent circuit with AVG, (c) negative half-line cycle HF equivalent circuit with AVG, and (d) positive half-line cycle high HF equivalent circuit with CCT.

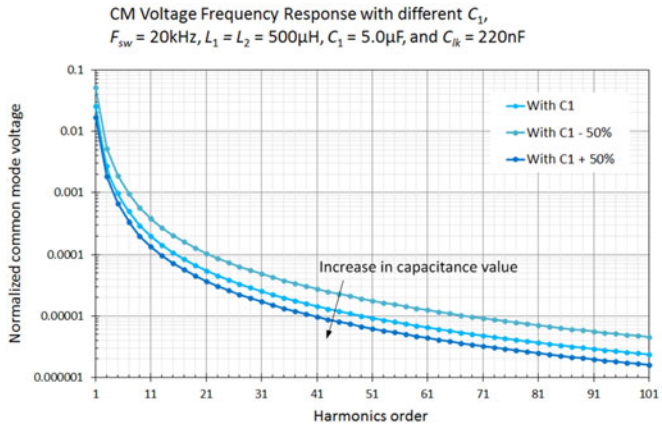

Fig. 4. Frequency response of normalized CM voltage with different C_1.

B. HF CM Voltage Attenuation

CM voltage is an important issue to be considered for many applications such as motor drives and PV inverters. Apart from high DM voltage attenuation capability, the proposed inverter is also providing high attenuation capability to CM voltage. As shown in Fig. 3(b) and (c), C_1 is connected in parallel with the leakage capacitor (C_{lk}), such as the parasitic capacitor across the ball bearing in a motor or across the frame and ground of a PV panel [9]. Therefore, the CM voltage, particular the HF component, is stabilized by C_1 and the HF CM current will be reduced accordingly. From HF signal's point of view, the AVG capacitor (C_1) and the ac grid source are low impedance elements, it seems that the negative terminal of the dc input (V_{in}) connects to the earth. Thus, the circuit is named AVG. The relationship between the normalized CM voltage and C_1 is given as

$$V_{hf_{\text{CM\_normalized}}} \leq \left| \frac{1}{1 - 0.5(n\omega_{\text{sw}})^2 L\,(C_{lk} + C_1)} \right|_{n\,=\,1,3,\ldots} \tag{1}$$

where ω_{sw} is angular switching frequency, by setting $L_1 = L_2 = L$, and n is the harmonic order of the HF switching voltage source v_a or v_b dependence on the polarity of the line voltage. Fig. 4 shows the graphical expression of (1), it can be seen that the attenuation to the HF CM voltage is higher with larger C_1. As a result, the HF CM current of the proposed inverter with AVG can be adjusted by the value of C_1.

C. GF Ground Leakage Current of a FB Inverter Using USS With AVG

AVG is not affecting the GF CM voltage of a typical FB with USS. Fig. 5 shows the equivalent circuits for investigating the GF CM voltage by shorting the inductors and opening the HF leg. C_{lk} is connected in parallel with the circuit that is highlighted in blue. Therefore, the total voltage across the blue paths show in Fig. 5(a) and (b) are the GF CM voltage across the C_{lk} in positive and negative half-line cycles, $v_{\text{CM\_GF\_AVG\_+ve}}$ and $v_{\text{CM\_GF\_AVG\_−ve}}$, respectively. The CM voltage can be described as follows:

For positive half-line cycle

$$v_{\text{CM\_GF\_AVG\_+ve}} = V_{\text{in}} - \widehat{V_{\text{ac}}} \sin \omega t \tag{2}$$

where $\widehat{V_{\text{ac}}}$ is peak value of grid voltage.

For negative half line cycle

$$v_{\text{CM}_{\text{GF}}\text{\_AVG\_}-ve} = V_{\text{in}}. \tag{3}$$

Fig. 6 shows the plot of GF CM voltage of FB inverter using USS with AVG by using (2) and (3). The GF CM voltage can be expressed as follows by the observation of Fig. 6:

$$v_{\text{CM\_GF\_AVG}} = V_{\text{in}} - \frac{\widehat{V_{\text{ac}}}}{2} \times \left(\frac{2}{\pi} + \sin \omega t - \frac{4}{\pi} \sum_{n\,=\,2,4,\ldots}^{\infty} \frac{\cos n\omega t}{n^2 - 1} \right). \tag{4}$$

The first, second, and third terms inside the bracket of (4) are the dc, the fundamental, and the even-order harmonics terms of the GF CM voltage, respectively. Derivative of (4) shows the GF ground leakage current

$$i_{\text{CM\_GF\_AVG}} = -\frac{\widehat{V_{\text{ac}}} C_{lk}}{2} \times \left(\omega \cos \omega t + \frac{4n\omega}{\pi} \sum_{n\,=\,2,4,\ldots}^{\infty} \frac{\sin n\omega t}{n^2 - 1} \right). \tag{5}$$

From (5), it can be seen that the ground leakage current is not affected by the proposed AVG circuit.

Fig. 3(d) shows the positive half-line cycle HF equivalent circuit of inverter with CCT. Considering the total capacitance of the filter capacitor is the same between AVG and CCT, in circuitry point of view, AVG and CCT give the same equivalent circuit toward the CM current. Therefore, both solutions give the same response to the CM current.

III. Simplified Design Guideline

In this section, a simplified design procedure of the AVG circuit is presented. It is basically governed by the required HF DM and HF CM current magnitudes.

A. Design of Output Filter Capacitor (C_1)

The output filter capacitor is designed according to the HF CM current limitation. By Fig. 3(c), it can be observed that the HF CM current can be determined as follows:

$$i_{\text{HF\_CM}}\ (t) = i_{L1}\ (t) - i_{L2}\,(t) - i_{C1}\,(t)\,. \tag{6}$$

The impedance of L_2 toward the HF CM current is much higher than C_{lk} and C_1, Δi_{L2} is assumed to zero for simplicity and without loss of generality. Therefore, C_1 and C_{lk} are connected in parallel as a current divider toward i_{L1}. The capacitance C_1 can be determined as follows:

$$\Delta i_{L1} = \Delta i_{\text{HF\_CM}} + \Delta i_{C1} \tag{7}$$

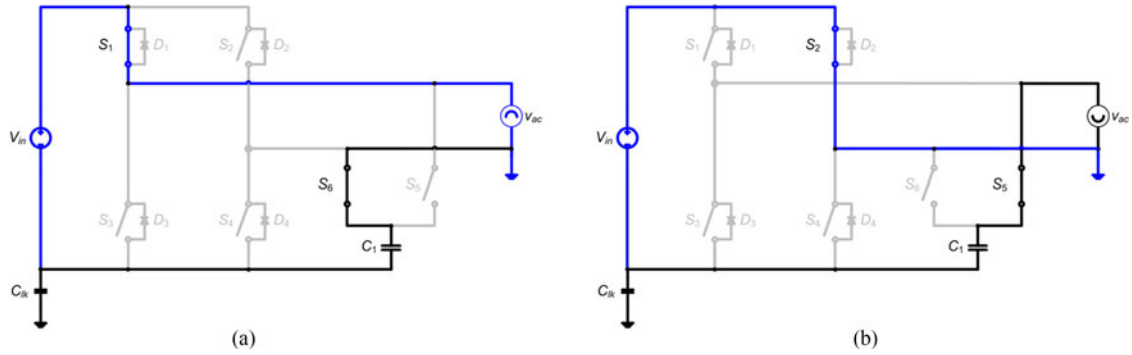

Fig. 5. Equivalent circuits for investigating the GF CM voltage. (a) Positive half-line cycle and (b) negative half-line cycle.

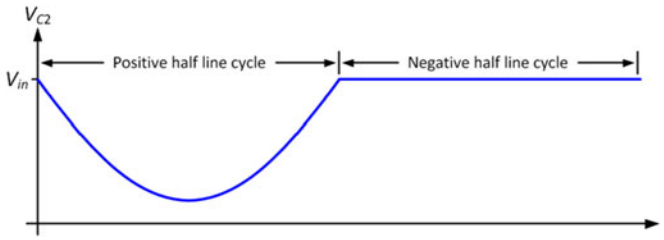

Fig. 6. GF CM voltage of FB USS AVG.

$$C_1 = C_{lk}\ \frac{\Delta i_{L1}}{\Delta i_{\mathrm{HF\_CM}}} - C_{lk}. \tag{8}$$

B. Design of Output Filter Inductors (L_1, L_2)

The output filter inductor is designed by considering the maximum allowable HF DM current ripple. By setting the grid-side HF DM current of FB with CCT equals to the one with AVG, and $L_1 = L_2 = L$

$$\Delta i_{\mathrm{CCT}}\ \frac{1}{2} = \Delta i_{\mathrm{AVG}} \frac{1}{1+\omega_{\mathrm{sw}}^2 LC_1}. \tag{9}$$

Δi_{CCT} is the inverter-side DM peak-to-peak current ripple magnitude of FB with CCT and USS. The grid-side DM current ripple magnitude is about half of the inverter side. Δi_{AVG} and $\Delta i_{\mathrm{AVG}} \frac{1}{1+\omega_{\mathrm{sw}}^2 LC_1}$ are the inverter-side and grid-side DM current ripple respectively of FB with AVG and USS.

By using (9)

$$\frac{v_{L_{\mathrm{CCT}}}}{L_{\mathrm{CCT}}}\Delta t\ \frac{1}{2} = \frac{v_{L_{\mathrm{AVG}}}}{L}\ \Delta t \frac{1}{1+\omega_{\mathrm{sw}}^2 L_{\mathrm{AVG}} C_1}. \tag{10}$$

$v_{L_{\mathrm{CCT}}}$ and $v_{L_{\mathrm{AVG}}}$ are the voltage across inverter-side inductor of inverters with CCT and AVG. By observing Fig. 3(b) and (d), it can be been that the $v_{L_{\mathrm{CCT}}}$ and $v_{L_{\mathrm{AVG}}}$ are the same, that is $v_{L_{\mathrm{CCT}}} = v_{L_{\mathrm{AVG}}}$. Therefore, the required inductance of FB with AVG can be determined as follows:

$$L^2 + \frac{L}{\omega_{\mathrm{sw}}^2 \mathrm{C}_1} - \frac{2\mathrm{L}_{\mathrm{CCT}}}{\omega_{\mathrm{sw}}^2 \mathrm{C}_1} = 0. \tag{11}$$

The change in permeability against magnetic field strength of the core material should be considered after determining required inductance. But it is out of the scope of this paper.

Fig. 7 shows a design example of the required inductance by using (11) with respect to the switching frequency for 1-kW, 110-V/60-Hz single-phase inverter with the AVG circuit and inverter with (CCT) [9] with 10% current ripple. The red line shows the minimum required total inductance, i.e., L_1 plus L_2, and the blue line shows the minimum required inductance for the one with CCT. For a 20-kHz switching frequency, the minimal total required inductance is 1.1 mH for AVG and 3.1 mH for CCT. This design results in a smaller inductor and lower cost. In case of keeping the same inductance between AVG and CCT at 3.1 mH, the switching frequency of the inverter with AVG can be reduced to 10 kHz for keeping the same HF DM ripple current magnitude. This design results in a lower switching loss. Hence, inverter with the proposed AVG circuit provides higher flexibility on the optimization of cost and efficiency.

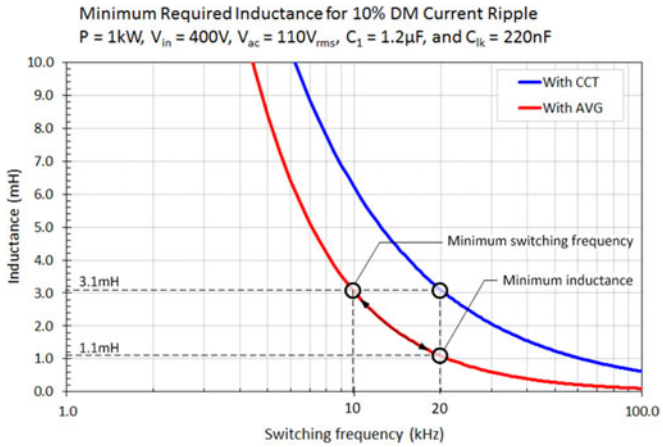

Fig. 7. Minimum required output filter inductance of inverters with AVG and with CCT.

IV. Benchmarking With Different Single-Phase Inverter Topologies and Its Variants

Table I shows a comparison of the proposed AVG topology to the other candidates which are used to solve CM voltage issue. It can be seen that the advantages of the proposed topology are as follows:

1) low conduction loss since only two semiconductor devices are creating losses in both power transfer and freewheeling modes as shown in the third column of Table II
2) high utilization of output filter inductors and higher order output filter structure without adding additional inductor

TABLE I
BENCHMARKING OF THE PRIOR SINGLE-PHASE GRID-CONNECTED INVERTERS

Inverter topology	No. of switches	No. of devices conduct in energy transfer or freewheeling states	O/P filter
HERIC [15]	6	transfer: 2, freewheeling: 2	*L*
Hybrid frequency phase legs [16]	4	transfer: 2, freewheeling:2	*L*
H5 [14]	5	transfer: 3, freewheeling: 3	*L*
H6 [18]	6	transfer: 4, freewheeling: 4	*L*
H6 type [17]	6	transfer: 3, freewheeling: 2	*L*
Neutral wire – PV panel direct connection [22]	6	transfer: 2, freewheeling: 2	*L*
Neutral wire – PV panel direct connection [24]	6	transfer: 3, freewheeling: 5 (equivalent)	*L*
Neutral wire – PV panel direct connection [23]	2	transfer: 2, freewheeling:2	*L*
Neutral wire – PV panel direct connection [25]	3	Positive half-line cycle: 1, negative half-line cycle: 3	*L*
NPC type [19]	6	transfer: 3, freewheeling: 2	*L*
The proposed inverter with AVG	6	transfer: 2, freewheeling:2	*LCL*

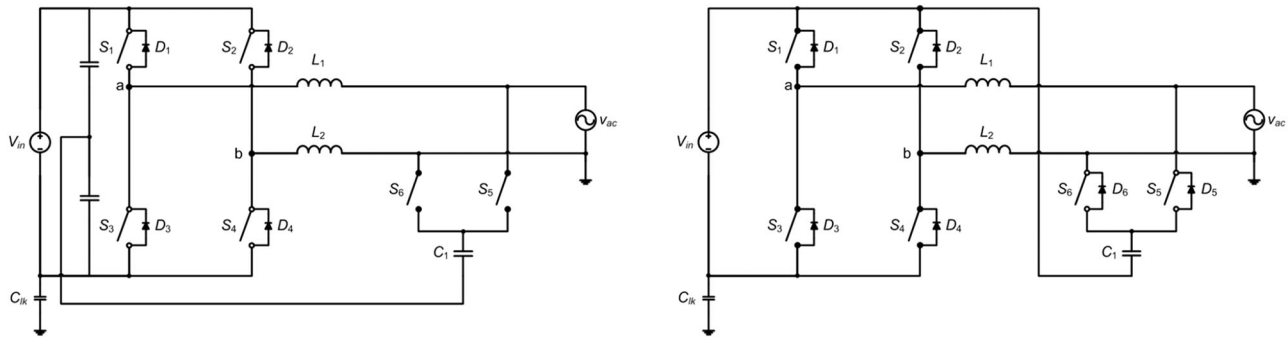

Fig. 8. Variants of the proposed inverter with AVG.

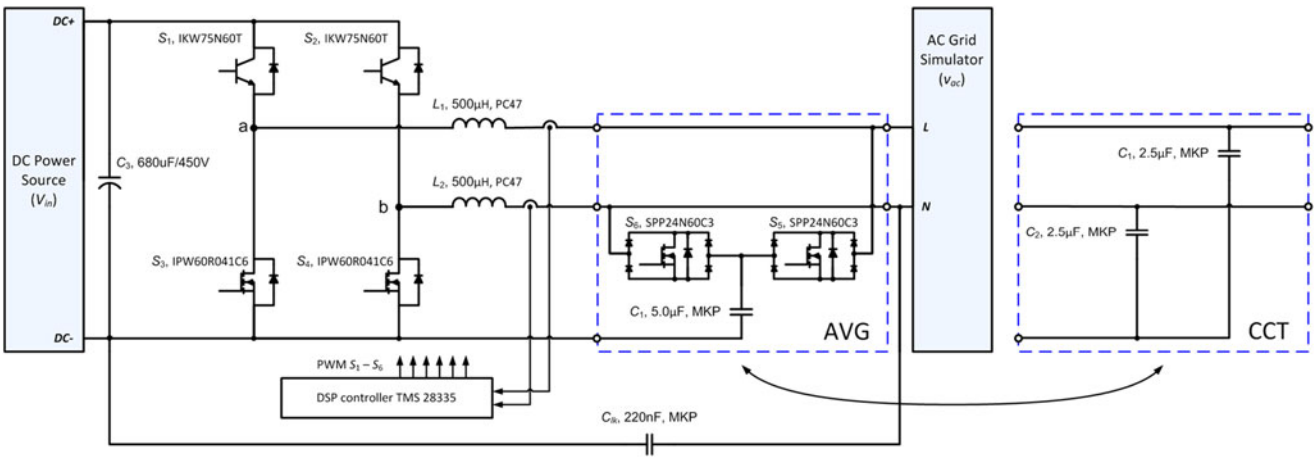

Fig. 9. Circuit diagram of the laboratory prototype and experimental set-up for inverter with AVG and CCT.

as shown in the fourth column, it results smaller inductance requirement for a specified DM current ripple;

3) no complicated additional control since the AVG's switches are switching at low frequency and synchronizing with the low-frequency main switches.

As a result, the proposed inverter can give high efficiency, small size of filter inductor and is simple in implementation.

The topology shown in Fig. 1 is one of the possible configurations of the proposed AVG in a single-phase FB inverter. By considering zero internal resistance of ideal voltage source, Fig. 8 shows the alternative configurations which give the same aforementioned electrical characteristics. The electrical performance of all these variants are the same except the dc voltage offset across C_1 since it is connecting to $V_{\rm in}$ minus, half $V_{\rm in}$, or $V_{\rm in}$ plus in the three variants.

V. SIMULATION AND EXPERIMENTAL RESULTS

In order to verify the HF DM and CM currents suppression capability of the proposed inverter with AVG; simulations have been ran in PLECS to study the performance between the

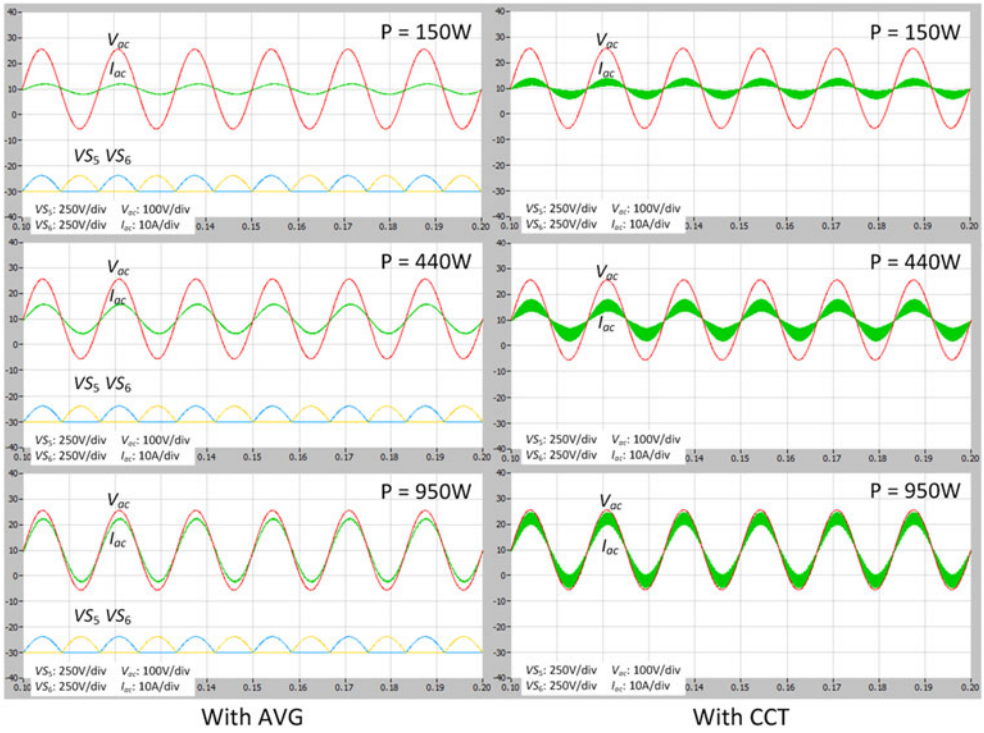

Fig. 10. Simulated steady-state output current waveforms of the inverters with AVG and CCT at 150, 440, and 950 W output.

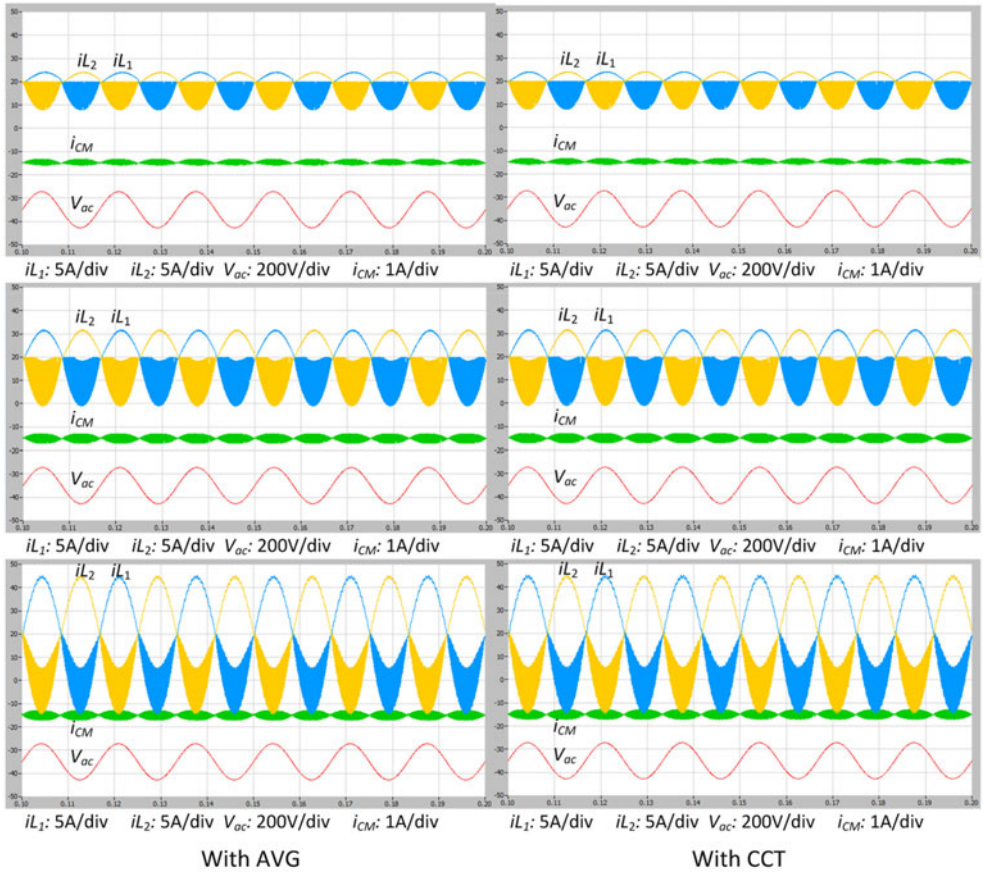

Fig. 11. Simulated steady-state output filter inductor currents and current waveforms of the inverters with AVG and CCT at 150, 440, and 950 W output and C_{lk} equals to 220 nF.

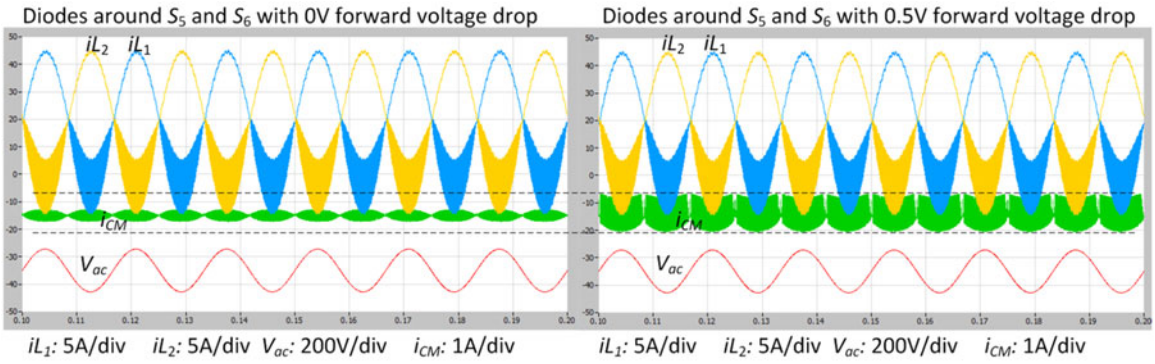

Fig. 12. Simulated CM current response refer to the forward voltage drop of the diodes around S_5 and S_6.

proposed AVG and the conventional CCT topologies. The value of the output filters, including the filter inductor and capacitor, are identical for the two topologies in this comparison. The corresponding experimental verifications are performed and the circuit diagram of the prototype is shown in Fig. 9. Fig. 10 shows the simulation results of both inverters with AVG and CCT at different output power. The output filter design is following the guideline presented in Section III and the values of *L* and *C* are shown in Fig. 9. The windows on the left show the simulation results of inverter with AVG and the right for CCT. It can be seen that the HF current ripple of the ac grid current is less than 0.5 A with AVG from 150 to 950 W output. On the contrary, it is ∼2.8 A at 150 W and ∼4.5 A at 440 W and 950 W for CCT. It verifies the high DM ripple current attenuation ability of the proposed AVG. Drain-source voltage across S_5 and S_6 are shown in Fig. 10 and it is equal to the ac grid voltage when the switch is in blocking state. Fig. 11 shows the simulation results of the output filter inductor currents, i_{L1} and i_{L2}, and the CM current, $i_{\rm CM}$, of the inverters with both AVG and CCT. It can be seen that the inductor current of both AVG and CCT are very similar. Therefore, it offers an opportunity to modify the existing inverter with CCT to AVG without changing the output filter inductors. The CM current of the inverter with CCT and AVG is the same as discussed in Section II-A. However, considering the forward voltage, V_f, drop across the diodes around S_5 and S_6, the diodes can be conducted unless high enough voltage, i.e., $2V_f$, has been built up across C_{lk} which leads to higher CM current. A simulation results is shown in Fig. 12 that the V_f of the diodes is 0.5 V. It can be seen that the CM current becomes higher for roughly three times. In order to lessen this issue, S_5 and S_6 can be implemented by back-to-back connected MOSFETs which has zero V_f.

A 1-kW, 400-V dc input and 110 Vrms/60-Hz ac output FB inverter with the proposed AVG circuit hardware prototype has been built for experimental verification. The inverter is switching with unipolar modulation at 20 kHz. The CCT counterpart is also tested on the same prototype for benchmarking. The circuit diagram and key components of the prototype are shown in Fig. 9. Due to the better switching performance of MOSFETs and antiparallel diode of IGBTs; MOSFETs are selected for S_3 and S_4 and IGBTs are selected for S_1 and S_2. IGBTs can also be used in S_3 and S_4 which give lower cost but higher

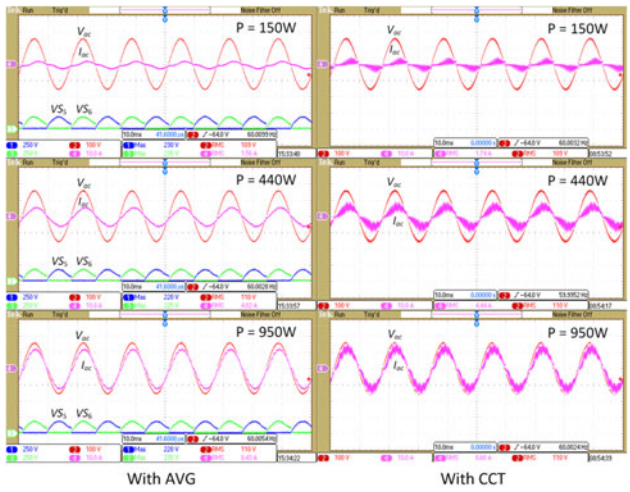

Fig. 13. Experimental steady-state output current waveforms of the inverters with AVG and CCT at 150, 440, and 950 W output.

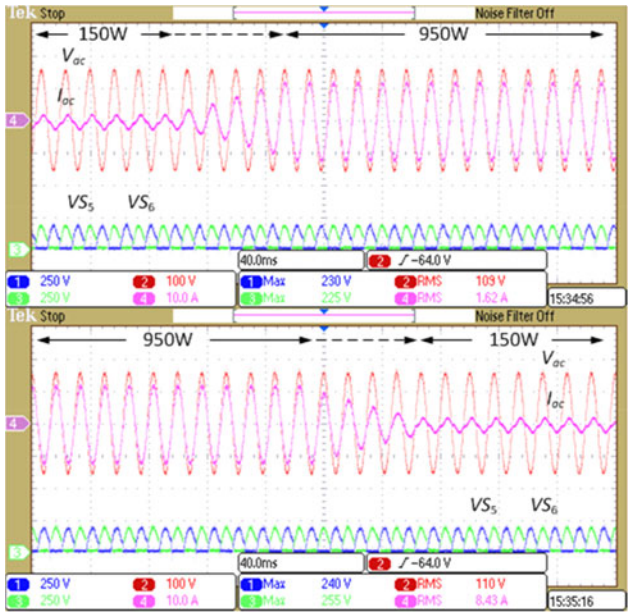

Fig. 14. Experimental dynamic power changes waveforms of the inverters with AVG from 150 to 950 W and from 950 to 150 W.

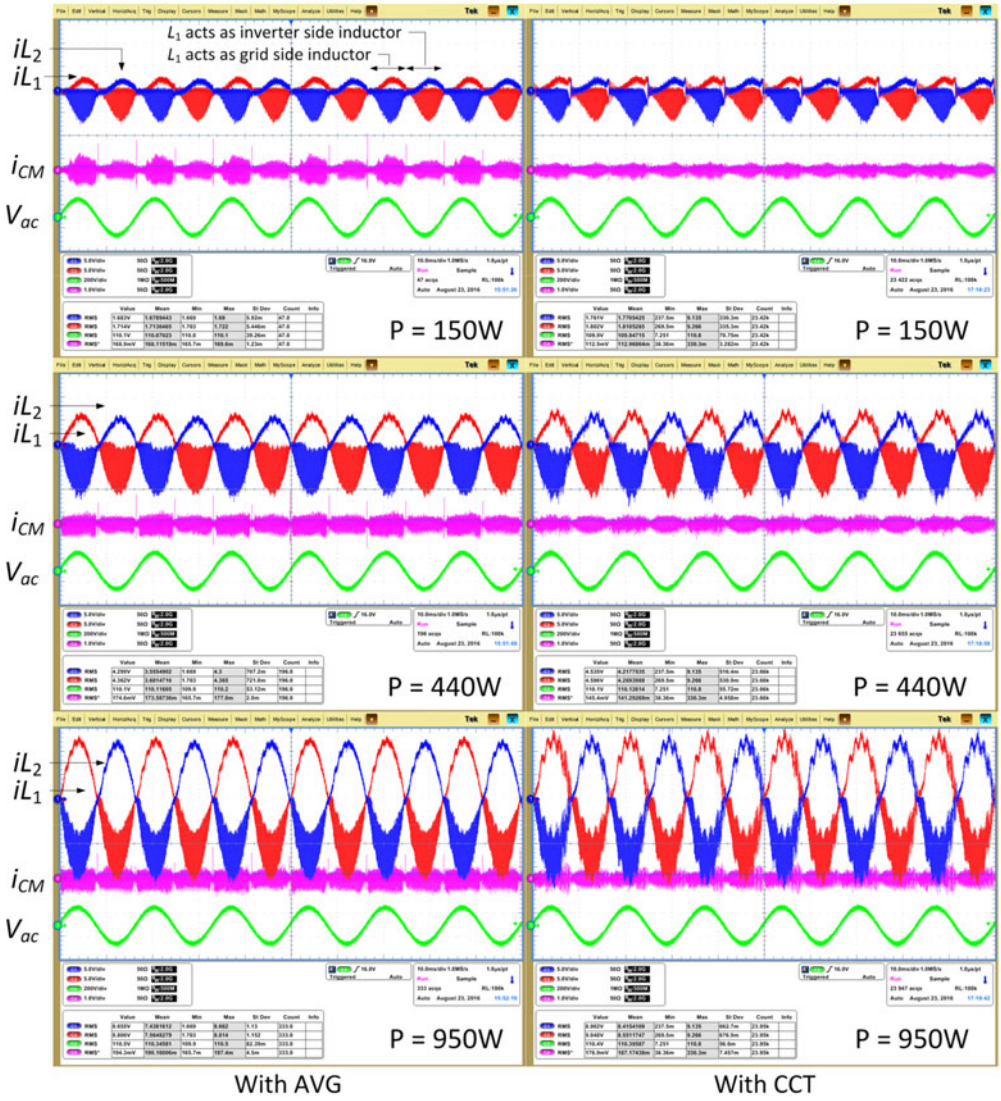

Fig. 15. Experimental steady-state output filter inductor currents and CM mode current waveforms of the inverters with AVG and CCT at 150, 440, and 950 W output and C_{lk} equals to 220 nF.

conduction and switching losses in general. The prototype was tested with 400-V dc input and 110-Vrms ac grid with both AVG and CCT configurations. Fig. 13 shows the experimental steady-state waveforms of both candidates at 150, 440, and 950 W output. It can be seen that the HF DM mode current ripple of the inverter with AVG is much smaller than the one with CCT from light load to heavy load. The HF current ripple of the ac grid current is less than 1.0 A with AVG from 150 to 950 W output. On the contrary, it is ∼2.8 A at 150 W and ∼6.0 A at 440 W and 950 W for CCT. The experimental results are matching with the simulation results which show in Fig. 10. Fig. 14 shows the dynamic power change waveforms of the proposed inverter with AVG between 150 and 950 W. It can be seen that the power is changing smoothly and the drain-source voltage across S_5 and S_6 is not subject to the power change as explained. Fig. 15 shows the inductor currents of L_1 and L_2 and the CM current across C_{lk}. Similar to the simulation results, the inductor acts as an inverter-side inductor, where the current ripple is larger; the current ripple is smaller when the inductor

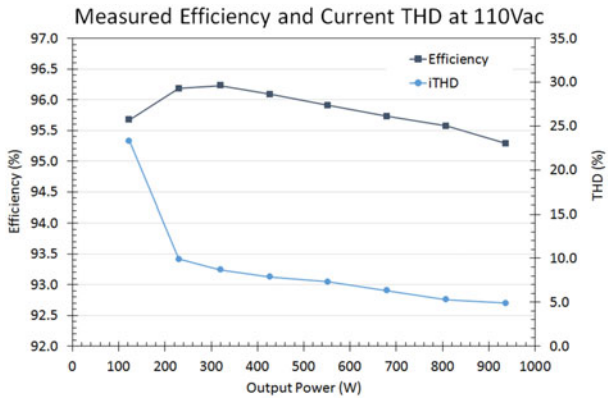

Fig. 16. Measured efficiency and current THD of the prototype with AVG.

acts as a grid-side inductor. The HF CM current is around 130 to 170 mA RMS, there is ∼50 mA measurement offset, where the C_{lk} is 220 nF. The HF CM current for AVG and CCT under

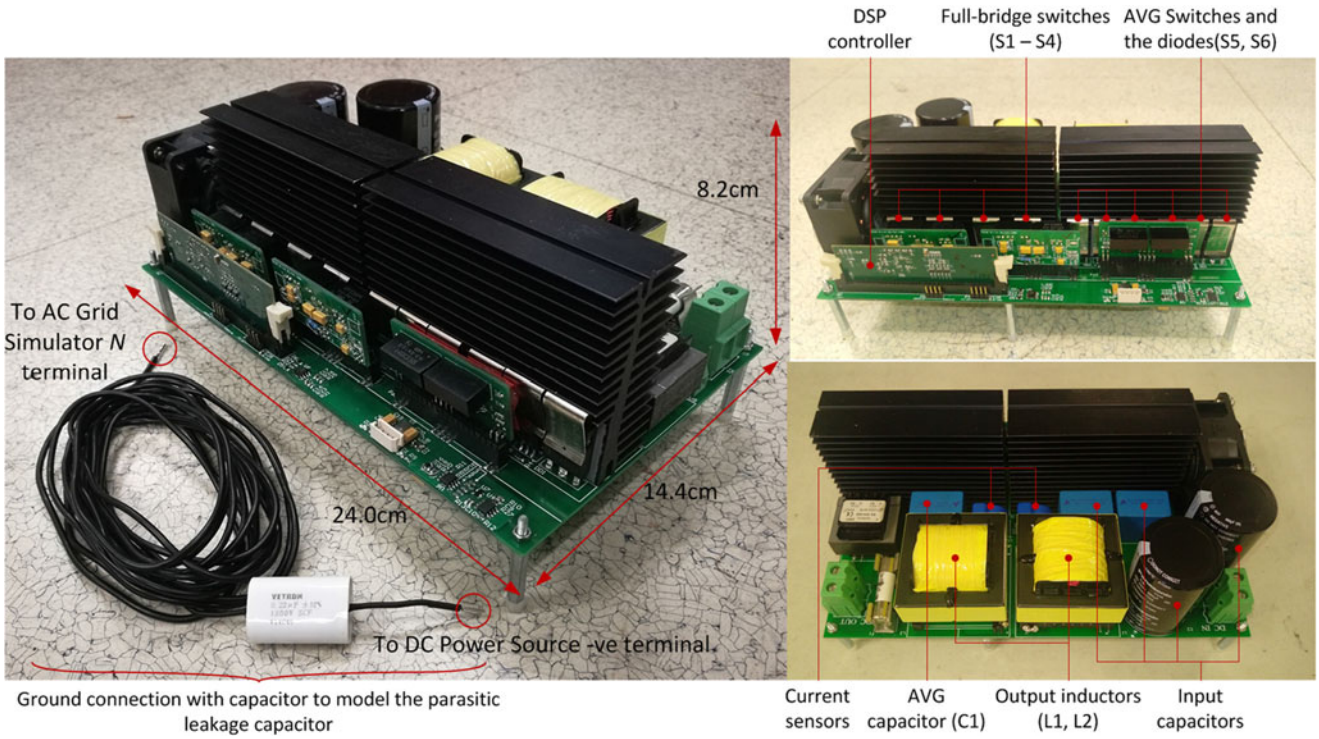

Fig. 17. Photos of the proposed inverter with AVG laboratory prototype.

the same conditions is around 200 and 180 mA RMS at 950 W output. It proves that the AVG topology can effectively suppress the CM currents. Apart from the low-frequency distortion in the results of inverter with CCT, the inductor current waveforms are very similar between inverter with AVG and with CCT. There is no observable difference in the current ripple magnitude in both positive and negative half-line cycles. It is in-line with the simulation results and no change on the inductor is required for changing the topology from CCT to AVG. A little higher in CM current in the case with AVG, it is due to the voltage drop across the diodes around S_5 and S_6 which is simulated and shown in Fig. 12. Fig. 16 shows the measured efficiency and THD of the proposed inverter with AVG, the maximum efficiency is around 96.4% at 250 W, it reaches 95.3% efficiency at rated power 950 W. According to the current waveforms in Fig. 15 and the KCL circuit theory, there is an 8-A peak-to-peak HF ripple current going through the AVG circuit and its RMS value is about 1.4 A. The overall semiconductor loss of the AVG circuit is $\sim$3 W. It is not significant for a 950 W inverter. Output current THD is smaller in higher output power, it is mainly due to the inductor current is in discontinuous conduction mode at light load. The THD equals to 4.9% at 950 W output. Fig. 17 shows the photos of the prototype, the dimension is 24.0 cm $\times$ 14.4 cm $\times$ 8.2 cm. All semiconductor switches are controlled by a digital signal processor (DSP). Two output filter inductors are designed as identical, and each inductor connects to one individual current sensor. This is because the operating modes of the inductors are changed in every half-line cycle; it requires individual inductor current feedback signals to control the semiconductor switches for shaping the output current.

The prototype demonstrated the concept and functionalities of the proposed AVG circuit applying to a grid-connected FB inverter. By using the same concept and the suggested design guideline, the rated power of inverter could be scaled up (e.g., 5 kW) or down (e.g., 300W) for different applications. The AVG circuit only has semiconductor conduction losses which are created by the HF ripple current. As long as the ripple current amplitude remains same, the loss of the AVG circuit will be quite consistent in the range of the rated power.

VI. Conclusion

The proposed single-phase FB grid-connected inverter with AVG circuit has been presented in this paper. The proposed topology provided a high attenuation ability on both HF DM current and HF CM current. The key merit is to change the output filter from *L* (First order) to *LCL* (Third order) structure by using additional low-frequency switching semiconductors instead of adding additional grid inductors. Thus, the grid current ripple amplitude or the required inductance can be reduced comparing to the conventional topologies. Besides one of the grid terminals (Neutral or Line) is always connected to the dc-link terminal with the AVG capacitor that mitigates the HF leakage current in the system. The operating principle and converter steady-state characteristics of AVG-VSI topology were studied. Besides, dynamic behaviors and simplified design guidelines of the proposed AVG-VSI topology were presented. The theoretical predictions were successfully verified by computer simulations and laboratory measurements with a good agreement.

VII. Appendix

Proof of (1)

$$V_{n\omega_{\rm sw}\_\rm normalized} = \left| \frac{\frac{1}{jn\omega(C+C_{lk})}}{\frac{jn\omega L}{2} + \frac{1}{jn\omega(C+C_{lk})}} \right|_{n=1,3,\ldots}$$

$$V_{n\omega_{\rm sw}\_\rm normalized} = \left| \frac{1}{1-0.5(n\omega_{\rm sw})^2 L\,(C_{lk}+C_1)} \right|_{n=1,3,\ldots}. \quad (1)$$

Proof of (4)

Fig. 6 shows the plot of GF CM voltage of FB inverter using USS with AVG by using (2) and (3)

$$v_{\rm CM\_GF\_AVG} = V_{\rm in} - \frac{\widehat{V_{\rm ac}}}{2}\left(\sin\omega t + |\sin\omega t|\right).$$

By Fourier analysis, $|\sin\omega t| = \frac{2}{\pi} - \frac{4}{\pi}\sum_{n\,=\,2,4,\ldots}^{\infty} \frac{\cos n\omega t}{n^2-1}$

$$v_{\rm CM\_GF\_AVG} = V_{\rm in} - \frac{\widehat{V_{\rm ac}}}{2} \times \left(\frac{2}{\pi} + \sin\omega t - \frac{4}{\pi}\sum_{n\,=\,2,4,\ldots}^{\infty} \frac{\cos n\omega t}{n^2-1}\right). \quad (4)$$

Proof of (8)

By (7)

$$\Delta i_{L1} = \Delta i_{\rm HF\_CM} + \Delta i_{L2} + \Delta i_{C1}$$

Set $\Delta i_{L2} = 0$,

$$\Delta i_{L1} = \Delta i_{\rm HF\_CM} + \Delta i_{C1}$$

$$\Delta i_{\rm HF\_CM} = \Delta i_{L1}\frac{C_{lk}}{C_1 + C_{lk}}$$

$$C_1 = C_{lk}\,\frac{\Delta i_{L1}}{\Delta i_{\rm HF\_CM}} - C_{lk}. \quad (8)$$

References

[1] J. M. Carrasco *et al.*, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002–1016, Jun. 2006.

[2] W. Jiang and B. Fahimi, "Active current sharing and source management in fuel cell–battery hybrid power system," *IEEE Trans. Ind. Electron.*, vol. 57, no. 2, pp. 752–761, Feb. 2010.

[3] C. Ho, V. Cheung, and H. Chung, "Constant-frequency hysteresis current control of grid-connected VSI without bandwidth control," *IEEE Trans. Power Electron.*, vol. 24, no. 11, pp. 2484–2495, Nov. 2009.

[4] Y. Chen and K. M. Smedley, "A cost-effective single-stage inverter with maximum power point tracking," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1289–1294, Sep. 2004.

[5] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, "A review of single-phase grid-connected inverters for photovoltaic modules," *IEEE Trans. Ind. Appl.*, vol. 41, no. 5, pp. 1292–1306, Sep./Oct. 2005.

[6] H. F. Xiao, K. Lan, and L. Zhang, "A quasi-unipolar SPWM full-bridge transformerless PV grid-connected inverter with constant common-mode voltage," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 3122–3132, Jun. 2015.

[7] M. Islam and S. Mekhilef, "Efficient transformerless MOSFET inverter for a grid-tied photovoltaic system," *IEEE Trans. Power Electron.*, vol. 31, no. 9, pp. 6305–6316, Sep. 2016.

[8] B. Yang, W. Li, Y. Gu, W. Cui, and X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.

[9] D. Dong, F. Luo, D. Boroyevich, and P. Mattavelli, "Leakage current reduction in a single-phase bidirectional AC–DC full-bridge inverter," *IEEE Trans. Power Electron.*, vol. 27, no. 10, pp. 4281–4291, Oct. 2012.

[10] Safety of Power Converters for Use in Photovoltaic Power Systems—Part 1: General Requirement, IEC Standard 62109-1-2007, 2007.

[11] Y. He, H. S. H. Chung, C. N. M. Ho, and W. Wu, "Use of boundary control with second-order switching surface to reduce the system order for deadbeat controller in grid-connected inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 2638–2653, Mar. 2016.

[12] S. Jahdi *et al.*, "An analysis of the switching performance and robustness of power MOSFETs body diodes: A technology evaluation," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2383–2394, May 2015.

[13] N. McNeill, K. Sheng, B. W. Williams, and S. J. Finney, "Assessment of off-state negative gate voltage requirements for IGBTs," *IEEE Trans. Power Electron.*, vol. 13, no. 3, pp. 436–440, May 1998.

[14] M. Victor, F. Greizer, S. Bremicker, and U. Hübler, "Method of converting a direct current voltage from a source of direct current voltage, more specifically from a photovoltaic source of direct current voltage, into a alternating current voltage," *US Patent US7411802 B2*, Dec 8, 2008.

[15] H. Schmidt, C. Siedle, and J. Ketterer, "DC/AC converter to convert direct electric voltage into alternating voltage or into alternating current," *US Patent US7046534 B2*, May 16, 2006.

[16] X. Li and G. Dai, "Transformer-free unilateral inductor grid-connected inverter circuit," *Chinese Patent CN102255331A*, Nov. 23, 2011.

[17] W. Yu, J. S. Lai, H. Qian, and C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated AC-module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.

[18] G. Senosiain *et al.*, "Single-phase circuit to condition and transform direct current electric power into alternating current electric power," *Eur. Patent EP2053730B1*, Jun. 17, 2015.

[19] B. Sven, F. Greizer, and M. Victor, "Inverter, more specifically for photovoltaic plants," *US Patent US7843714 B2*, Nov. 30, 2010.

[20] G. Escobar, N. Ho, and S. Pettersson, "Method and apparatus for zero sequence damping and voltage balancing" *US Patent US9030854 B2*, May 12, 2015.

[21] Y. He, H. Chung, C. Ho, and W. Wu, "Modified cascaded boundary-deadbeat control for a virtually-grounded three-phase grid-connected inverter with LCL filter," *IEEE Trans. Power Electron.*, early access, 2016.

[22] J. Hantschel, "An inverter circuit for widening the input voltage range" *German Patent DE102006010694B4*, Mar. 8, 2006.

[23] P. Zacharias, J. Friebe, F. Blumenstein, A.-K. Gerlach, J. Scheuermann, and M. Zin, "Inverter," *US Patent US7813153B2*, Oct. 12, 2010.

[24] P. Zacharias and B. Sahan, "Inverter for feeding electric energy into a power system," *US Patent US8391038 (B2)*, Mar. 5, 2013.

[25] W. Richard, "Monopolar DC to bipolar to AC converter," *US Patent US7064969B2*, Aug. 26, 2004.

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